

13247

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

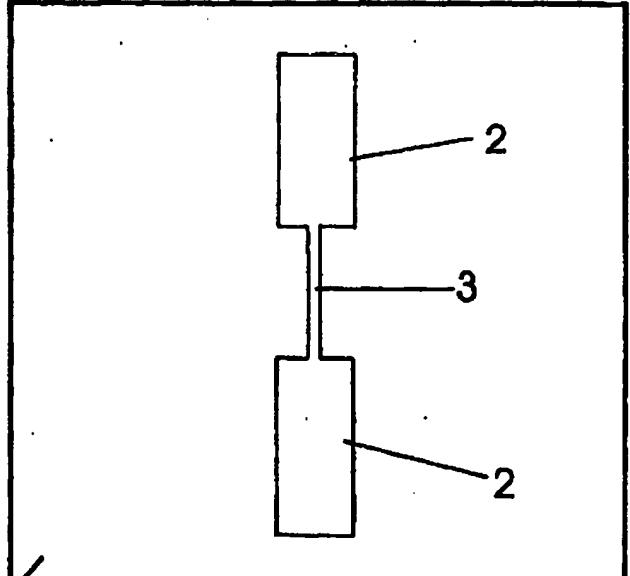
(51) International Patent Classification 6 : H05K 1/16	A1	(11) International Publication Number: WO 99/45753
		(43) International Publication Date: 10 September 1999 (10.09.99)

(21) International Application Number: PCT/SE99/00325	(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SB, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).
(22) International Filing Date: 5 March 1999 (05.03.99)	
(30) Priority Data: 9800707-3 5 March 1998 (05.03.98) SE	
(71) Applicant (for all designated States except US): ETCHTECH SWEDEN AB (SE/SE) ; Per Albin Hanssons väg 41, S-205 12 Malmö (SE).	
(72) Inventor; and	
(73) Inventor/Applicant (for US only): WIKSTRÖM, Bo (SE/SE) ; Jakutigen 10, S-261 75 Asmundtorp (SE).	
(74) Agent: AWAPATENT AB ; P.O. Box 5117, S-200 71 Malmö (SE).	
	Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments. In English translation (filed in Swedish).

(54) Title: METHOD FOR MANUFACTURING A RESISTOR

(57) Abstract

A method for manufacturing a resistor function in an electric conductor on the surface of a carrier, preferably a conductor on printed circuit boards, substrates and chips. By etching using an anisotropic etching technique, the conductor is provided with at least one portion which has a smaller cross-sectional area than the conductor surrounding the portion, the length and width of the portion being such that a predetermined resistance is obtained in the conductor. A resistor according to the invention is on both sides connected to a conductor on a carrier, such as a printed circuit board, a substrate or a chip. The resistor comprises a conductor portion positioned on the carrier and having a significantly smaller cross-sectional area than the conductor on both sides of the resistor.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LJ	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

METHOD FOR MANUFACTURING A RESISTOR

Field of the Invention

The present invention relates to a resistor and a method for manufacturing a resistor on carriers, preferably printed circuit boards, substrates and chips with or 5 without integrated circuits, in the field of electronics.

Background Art

Printed circuit boards, substrates or chips have conductor structures on their surfaces or inside to connect other components, integrated functions or to connect 10 to the surroundings. If resistor components are required, they are mounted as discrete components or applied as resistor pastes to printed circuit boards, substrates or chips so as to achieve the necessary resistance.

This is a time-consuming and complicated process. 15 Therefore there is a need for a process which facilitates the manufacture of resistors.

Summary of the Invention

An object of the present invention is to overcome the above drawbacks and render the realisation of the 20 resistor function in electronic products such as printed circuit boards, substrates and chips more effective.

These objects are achieved by a resistor and a method according to the appended claims.

A method for manufacturing a resistor function in 25 an electric conductor on the surface of a carrier, preferably conductors on printed circuit boards, substrates and chips, according to the invention is characterised in that the conductor, by etching using an anisotropic etching technique, is provided with at least one portion 30 which has a smaller cross-sectional area than the conductor on both sides of the portion, the length and width of the portion being such that a predetermined resistance is obtained in the conductor.

A resistor which on both sides is connected to a conductor on a carrier, such as a printed circuit board, a substrate or a chip, according to the invention is characterised in that the resistor comprises a conductor 5 portion which is positioned on the carrier and which has a significantly smaller cross-sectional area than the conductor on both sides of the resistor.

By a significantly smaller cross-sectional area is meant that the cross-sectional area is smaller than 20%, 10 preferably smaller than 5% of the cross-sectional area of the conductor.

A method according to the invention is based on the use of an anisotropic etching technique to generate conductor structures having a desired resistance.

15 By the resistor function being achieved by the conductor being provided with a portion of a smaller cross-sectional area, the resistor function can be made at the same time as the conductor structure on, for instance, a printed circuit board is made.

20 By the forming of the resistor function according to a preferred embodiment occurring in the normal conductor path, the resistor function can also be integrated in the internal conductor layers in multilayer printed circuit board or substrates, which causes improved distribution 25 of the thermal energy generated by the resistor function.

According to a preferred embodiment of the present invention, the reduced cross-sectional area is a reduction of the width of the conductor in the plane of the surface. The desired resistance is then obtained by an 30 adaptation of the width of the conductor or by adaptation of the length of the narrowed portion.

The conductors are preferably formed with a narrowed portion which has been etched by an anisotropic etching technique, to such a conductor width that such a noticeable resistance level is obtained that other resistor 35 functions are not necessary in the extent of the conduc-

tor path between the other component connections to which an applied resistor function would have been connected.

According to an alternative embodiment of the present invention, the reduced cross-sectional area is provided by at least one essentially longitudinal groove being etched in the surface of the conductor. If the grooves are etched through the entire conductor, at least two essentially parallel conductors are obtained.

A person skilled in the art realises that the anisotropic etching technique is selected among known anisotropic etching techniques. The specific application determines which etching technique is to be chosen. Examples of anisotropic etching techniques are reactive ion etching, plasma etching and different kinds of wet etching.

According to a preferred embodiment of the present invention, use is made of a wet etching technique. This is advantageous from the viewpoint of costs.

According to a special aspect of the invention, use is made of a chemically etching etching fluid, in which the etchant, which constitutes the active substance, is present in a diluted solution. Extremely good results can be produced, such as exact etchings in small dimensions. This aspect of the invention is based on the surprising discovery that an etching fluid which has been diluted to have a negligible etching effect can be used for anisotropic etching under the action of an electric field.

This results in etching of an electrically conductive etching material by means of an etchant, which is present in a solution which is diluted to such a great extent as not to be practically usable for chemical etching. The etchant concentration is so low that such reactions between the etchant and the etching material as result in the removal of atoms from the etching material occur only sporadically. By an electric field being produced in the etchant solution between the electrode and a surface portion of the etching material, a local con-

centration of etchant forms on the surface portion of the etching material. This results in a pronounced increase of the etching rate of the etchant while at the same time the etching direction of the etchant is affected.

5 The described etching method is known from PCT Application SE97/01480.

If exact resistors are to be manufactured, it is advantageous to measure the resistance of the conductor during etching. When the measured resistance conforms 10 with the desired value, the etching is interrupted.

The above features can, of course, be combined in the same embodiment.

In order to further elucidate the invention, detailed 15 embodiments thereof will be described below, without the invention, however, being considered to be restricted thereto.

Brief Description of the Drawings

Fig. 1 illustrates a conductor on a printed circuit board, said conductor having a narrowed portion along 20 part of the length of the conductor path, according to an embodiment of the invention.

Fig. 2 illustrates a conductor on a printed circuit board, said conductor having a plurality of parallel conductor portions along part of the length of the conductor path, according to an alternative embodiment of 25 the invention.

Fig. 3 illustrates a conductor on a chip, said conductor having a portion with a conductor which is narrower than the surrounding conductor portions and which is 30 longer than the distance between the surrounding conductor portions.

Detailed Description of the Invention

Fig. 1 shows a printed circuit board, substrate or chip 1 which has a conductor 2 with a narrowed portion 35 3 to provide the intended resistance in the conductor. As a result, no separate resistor component or resistor

pressure is required. The length and width of the narrowed portion have been adapted to produce the desired resistor. In the Figure, the narrowed portion has the same width over its entire length, but a person skilled 5 in the art realises that the width may vary over the length.

Fig. 2a shows a printed circuit board, substrate or chip 1 which is provided with a conductor 4. Fig. 2b is a sectional view along line A-A in Fig. 2a. This is formed 10 with etched grooves 6, which results in the conductor 2 having narrowed conductor portions 5. This, in turn, results in the desired resistance value while at the same time the distribution of current in a plurality of conductors distributes the generation of power on a larger 15 surface. In the Figure, the grooves are etched through the thickness of the entire conductor, but alternatively the grooves extend only partly through the thickness of the conductor.

Fig. 3 illustrates a printed circuit board, substrate or chip 1 which is provided with one or more conductors 2. The conductor or conductors have been formed 20 with a narrowed conductor portion 3 which has such a great narrowing 3 in a conductor pattern prolonged in relation to the distance between the conductor paths 25 which are not narrowing, in order to increase the resistance value.

By thus increasing the length of the conductor, the width can be greater for a certain predetermined resistance compared with the case where the conductor is made 30 straight. The narrowed conductor portion has been distributed over a larger surface, which means that the generation of power is distributed on a larger surface, which in turn leads to a lower temperature of the conductor.

35 The conductor structure in Fig. 3 has been produced by masking and etching.

The embodiments described above are only to be regarded as examples. A person skilled in the art realises that the above embodiments can be varied in a number of ways without deviating from the inventive idea.

CLAIMS

1. A method for manufacturing a resistor function in an electric conductor on the surface of a carrier, preferably a conductor on printed circuit boards, substrates and chips, characterised in that the conductor, by etching using an anisotropic etching technique, is provided with at least one portion which has a smaller cross-sectional area than the conductor surrounding the portion, the length and width of the portion being such that a predetermined resistance is obtained in the conductor.
2. A method as claimed in claim 1, characterised in that the conductor is provided with a plurality of parallel portions whose total cross-sectional area is smaller than the cross-sectional area of the surrounding conductor.
3. A method as claimed in claim 1, characterised in that a portion of the conductor is etched by using an anisotropic etching technique so that said portion obtains a greater length and a smaller width than the original portion.
4. A method as claimed in claim 1, characterised in that the reduced cross-sectional area consists of a reduction of the width of the conductor in the plane of the surface.
5. A method as claimed in any one of claims 1, 2, 3 or 4, characterised in that the anisotropic etching is a wet etching method, and that it further comprises the step of performing anisotropic etching by arranging an electric field in the etching fluid adjacent to the conductor, the etching fluid being present in such a diluted solution that it is not capable of etching the conductor without an electric field, but in concentrated form etches the conductor without an electric field.

6. A method as claimed in any one of the preceding claims, characterised by the steps of measuring the resistance of the conductor during etching, and

5 interrupting the etching when the measured resistance corresponds to the predetermined resistance.

7. A method as claimed in any one of the preceding claims, characterised in that the conductor is coated with a further layer.

10 8. A resistor which on both sides is connected to a conductor on a carrier, such as a printed circuit board, a substrate or a chip, characterised in that the resistor comprises a conductor portion which is positioned on the carrier and which has a significantly smaller cross-sectional area than the conductor on both sides of the resistor.

15 9. A resistor as claimed in claim 8, wherein the conductor portion of the resistor has been given a smaller cross-sectional area by anisotropic etching.

20 10. A resistor as claimed in claim 8 or 9, characterised in that the conductor portion with a significantly smaller cross-sectional area consists of a plurality of parallel conductors whose total cross-sectional area is smaller than that of the surrounding conductor.

25

1/3

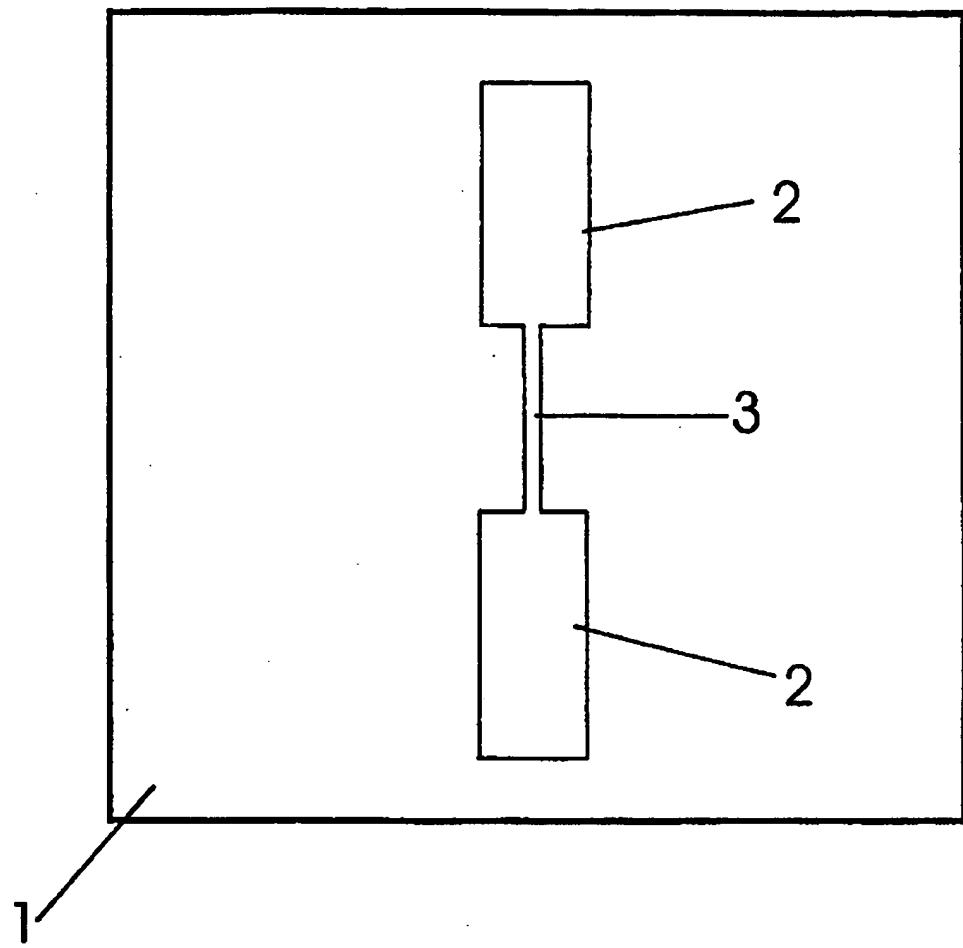
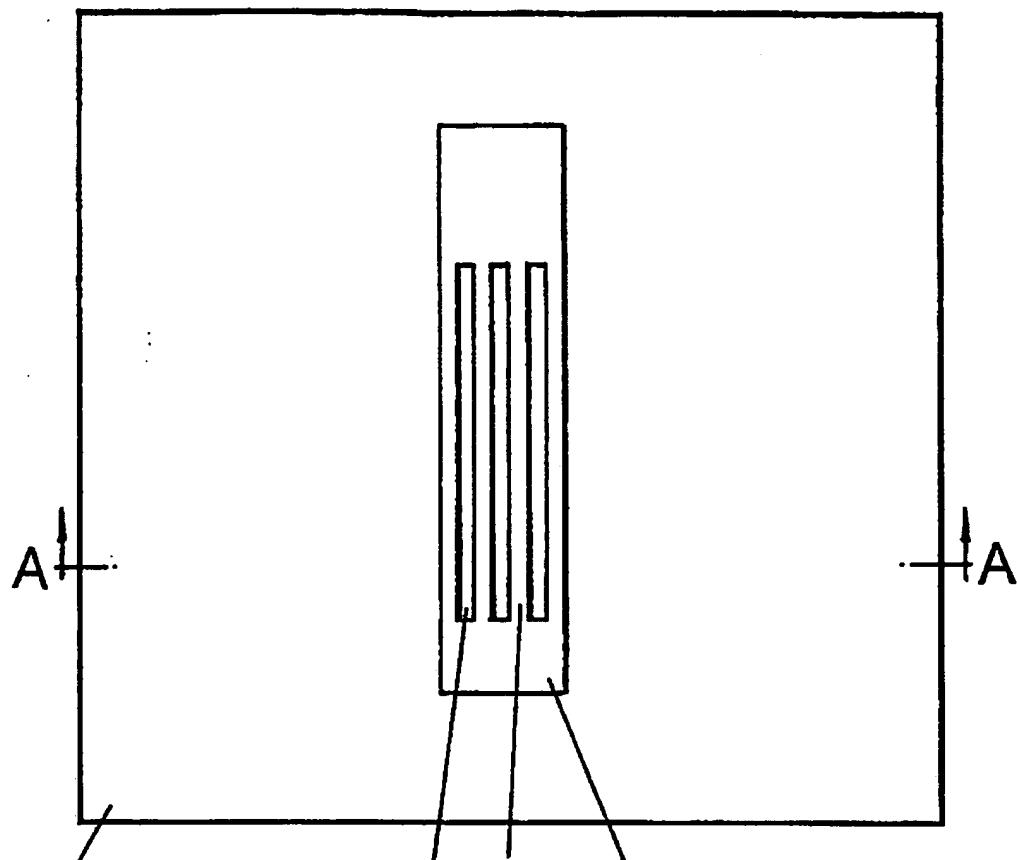


Fig. 1.

2/3

Fig. 2.a



A-A

Fig. 2.b

3/3

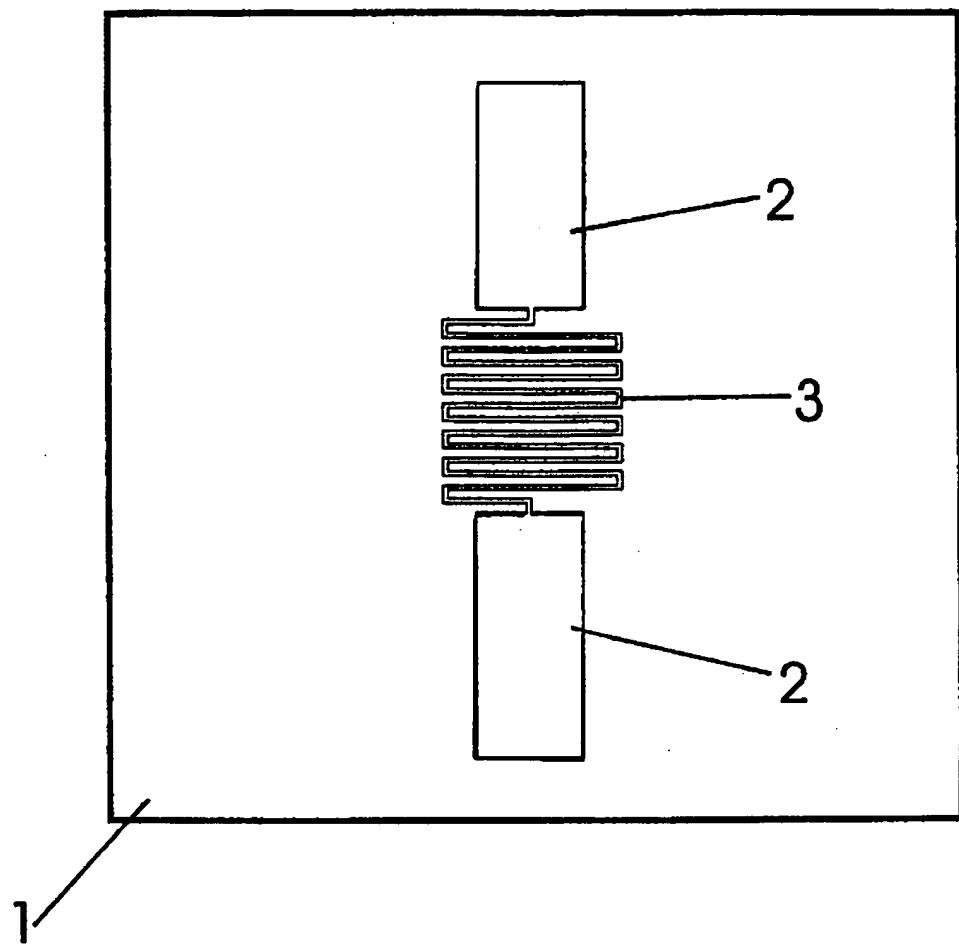


Fig. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 99/00325

A. CLASSIFICATION OF SUBJECT MATTER		
IPC6: H05K 1/16 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
IPC6: H05K, H01L, H01C Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched SE, DK, FI, NO classes as above		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0163760 A2 (NIPPON MEKTRON LTD.), 11 December 1985 (11.12.85) --	1-10
A	EP 0719079 A1 (KANTO KASEI CO., LTD.), 26 June 1996 (26.06.96) --	1-10
A	IBM Technical Disclosure Bulletin, Volume 33, No 10A, March 1991; "DECOUPLING CAPACITOR INCORPORATED IN PRINTED CIRCUIT BOARD" --	1-10
P, A	EP 0837623 A1 (MACDERMID INCORPORATED), 22 April 1998 (22.04.98) --	1-10
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
<ul style="list-style-type: none"> * Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "B" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&" document member of the same patent family</p>		
Date of the actual completion of the international search 5 July 1999	Date of mailing of the international search report 12 -07- 1999	
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. + 46 8 666 02 86	Authorized officer Marianne Bratsberg/MP Telephone No. + 46 8 782 25 00	

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE 99/00325

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	WO 9810121 A1 (OBDUCAT AKTIEBOLAG), 12 March 1998 (12.03.98) -----	1-10

INTERNATIONAL SEARCH REPORT
Information on patent family members

01/06/99

International application No.
PCT/SE 99/00325

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP 0163760 A2	11/12/85	NONE		
EP 0719079 A1	26/06/96	JP	8228064 A	03/09/96
EP 0837623 A1	22/04/98	JP	10135608 A	22/05/98
WO 9810121 A1	12/03/98	AU	4141697 A	26/03/98
		SE	508155 C	07/09/98
		SE	9603260 A	07/03/98